Patent claims

1. Method for producing a semiconductor device with the steps of:

applying an interconnect level (11, 12) to a semiconductor substrate (10);

structuring the interconnect level (11, 12); and

applying a solder layer (13) on the structured interconnect level (11, 12) in such a way that the solder layer (13) assumes the structure of the interconnect level (11, 12).

2. Method according to claim 1, characterized in that the interconnect level (11, 12) is applied in a sputtering process or in a depositing process without external current.

3. Method according to claim 1 or 2, characterized in that the interconnect level (12) which is applied comprises a metal, preferably copper and/or nickel and/or aluminum.

4. Method according to one of the preceding claims, characterized in that the interconnect level (11, 12) is structured with the aid of a photolithographic process.

5. Method according to one of the preceding claims, characterized in that a carrier layer (11) which preferably comprises titanium and is structured like the interconnect level (12) is applied on the semiconductor substrate (10).

6. Method according to one of the preceding claims, characterized in that the solder layer (13) is

applied in a printing process and is distributed in a predetermined way by re-liquefying or reflowing of the solder.

7. Method according to one of the preceding claims, characterized in that the solder layer (13) is applied in a dip soldering process, in which the upper side of the semiconductor substrate (10) provided with the structured interconnect level (11, 12) is dipped into a solder bath.

8. Method according to one of the preceding claims, characterized in that a solder resist layer is selectively applied on predetermined portions of the arrangement after the structuring of the interconnect level (11, 12) and before the application of the solder layer (13).

9. Method according to one of the preceding claims, characterized in that side walls (16) of the structured interconnect level (11, 12) and/or of the carrier layer (11) are wetted with solder.

10. Method according to one of the preceding claims, characterized in that both solder traces and solder balls (30) for the bonding of further semiconductor devices and/or a printed circuit board in the vertical direction are formed during the application of the solder layer (13), preferably in the same process step.

11. Method according to one of the preceding claims, characterized in that, after the application of the structured solder layer (13), a non-conductive plastic, preferably polymer, is applied in such a way that the tips of the solder balls (30) for the vertical bonding protrude from the plastic, other solder structures being covered over.

12. Method according to claim 11, characterized in that the applied polymer is only cured during or after the electrical bonding with a further semiconductor device and/or a printed circuit board in the vertical direction.

13. Method according to claim 11 or 12, characterized in that the polymer is applied in a printing process.

14. Method according to one of the preceding claims, characterized in that the conductive interconnect level (12) is formed on the semiconductor substrate (10) and/or contact devices such as bonding pads in a printing or stamping process with a highly reactive substance, which comprises at least one noble metal, such as preferably platinum or palladium.

15. Semiconductor device with:

a semiconductor substrate (10);

a structured interconnect level (11, 12) on the semiconductor substrate (10); and

a solder layer (13) on the structured interconnect level (11, 12) for enlarging the conductive cross section, the solder layer (13) assuming the structure of the interconnect level (11, 12).

16. Semiconductor device according to claim 15, characterized in that the structured interconnect level (12) comprises a metal, in particular aluminum and/or copper.

17. Semiconductor device according to claim 15 or 16, characterized in that the structured interconnect level (11, 12) provides on the semiconductor substrate (10) a carrier layer (11), which is structured like the interconnect level (12) and preferably comprises titanium and/or copper.

18. Semiconductor device according to one of claims 15 to 17, characterized in that side walls (16) of the structured interconnect level (11, 12) and/or of the carrier layer (11) are wetted with solder.

19. Semiconductor device according to one of claims 15 to 18, characterized in that the semiconductor device is mechanically connected to at least one further semiconductor device and/or a printed circuit board by means of a plastic or a polymer, the electrical connection being provided in the vertical direction by means of solder balls (30).

20. Semiconductor device according to one of claims 15 to 19, characterized in that the structured solder layer (13) has a solder layer height (14, 24) which corresponds approximately to half the structure width (15, 25) of the structured interconnect level (12).